

**Advance Information: AI1011**

**40W Power Packaged Transistor**  
**GaN HEMT on SiC**



UMS's CHK040A is an unmatched Packaged Gallium Nitride High Electron Mobility Transistor. It offers a general purpose and broadband solution for a variety of RF power applications.

It operates at high voltage (50V) and takes all the GaN key advantages such as high power (>40W), high PAE (55%) and wide band capability up to a frequency of 3GHz, compatible with both Pulsed and CW operation modes.

It is proposed in a low parasitic, low thermal resistance package, and requires an external matching circuitry.

The CHK040A is well suited for multi-purpose applications such as radar and telecommunication.

It is developed on a 0.5 $\mu$ m gate length GaN HEMT process, and is available as a ceramic-metal flange power package compliant with the RoHs and REACH directives.

## Recommended DC Operating Ratings

T<sub>case</sub>= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V <sub>DS</sub>	Drain to Source Voltage		50		V	
V <sub>GS_Q</sub>	Gate to Source Voltage		-1.3		V	V <sub>D</sub> =50V, I <sub>D_Q</sub> =300mA
I <sub>D_Q</sub>	Quiescent Drain Current		0.3	1	A	V <sub>D</sub> =50V
I <sub>D_MAX</sub>	Drain Current		2		A	V <sub>D</sub> =50V, compressed mode
I <sub>G_MAX</sub>	Gate Current (forward mode)		0	20	mA	Compressed mode

## DC Characteristics

T<sub>case</sub>= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V <sub>P</sub>	Pinch-Off Voltage	-3	-2	-1	V	V <sub>D</sub> =50V, I <sub>D</sub> = I <sub>DSS</sub> /100
I <sub>D_SAT</sub>	Saturated Drain Current		8		A	V <sub>D</sub> =7V, V <sub>G</sub> =2V
I <sub>G_leak</sub>	Gate Leakage Current (reverse mode)	-10			mA	V <sub>D</sub> =50V, V <sub>G</sub> =-7V
V <sub>B_DS</sub>	Drain-Source Break-down Voltage		200		V	V <sub>G</sub> =-7V, I <sub>D</sub> =20mA
R <sub>TH</sub>	Thermal Resistance		2		°C/W	

## RF Characteristics

T<sub>case</sub>= +25°C, CW mode, F = 3GHz

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
G <sub>SS</sub>	Small Signal Gain		15		dB	V <sub>D</sub> =50V, I <sub>D_Q</sub> =300mA
P <sub>SAT</sub>	Saturated Output Power		50		W	V <sub>D</sub> =50V, I <sub>D_Q</sub> =300mA
PAE	Max Power Added Efficiency		55		%	V <sub>D</sub> =50V, I <sub>D_Q</sub> =300mA
G <sub>PAE_MAX</sub>	Associated Gain at Max PAE		12		dB	V <sub>D</sub> =50V, I <sub>D_Q</sub> =300mA

These values are the intrinsic performance of the packaged device. They are deduced from measurements and simulations. They are considered in the reference plane defined by the leads of the package, at the connection interface with the PCB. The typical performance achievable in more than 25% frequency band around 3GHz was demonstrated using the reference board 61499547 presented hereafter.

### Advanced Information

## Absolute Maximum Ratings

$T_{case} = +25^{\circ}\text{C}$  <sup>(1), (2), (3)</sup>

Symbol	Parameter	Rating	Unit	Note
$V_{DS}$	Drain-Source Voltage	175	V	$V_G = -7\text{V}$ , no RF
$V_{GS\_Q}$	Gate-Source Voltage	-10, +2	V	
$I_{G\_MAX}$	Maximum Gate Current	40	mA	
$P_{IN}$	Maximum Input Power	39	dBm	
$T_{STG}$	Storage Temperature	-55 to +150	$^{\circ}\text{C}$	
$T_{Case}$	Case Operating Temperature	See note	$^{\circ}\text{C}$	(4)

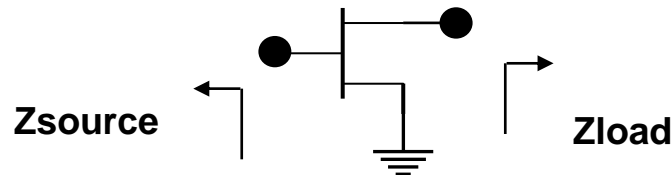
<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage.

<sup>(2)</sup> Duration < 1s.

<sup>(3)</sup> The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.

<sup>(4)</sup> See also the power dissipation characteristic

## Simulated Source and Load Impedance



Frequency (MHz)	Source	Load
500	1.9 - j3	15.5 + j14.4
1000	4 - j0.8	13.8 + j12.7
2000	2.2 - j6	5.2 + j7.5
3000	2.7 - j6.9	3 + j2.3

These values are given in the reference plane defined by the connection between the transistor leads and the PCB. A gap of 200 $\mu\text{m}$  is considered between the edge of the transistor and the PCB.

## Advanced Information

## Typical S-parameters

Tcase= +25°C, CW mode, V<sub>D</sub>=50V, I<sub>D,Q</sub>=300mA

Freq (GHz)	mag(S(1,1))	phase(S(1,1))	mag(S(2,1))	phase(S(2,1))	mag(S(1,2))	phase(S(1,2))	mag(S(2,2))	phase(S(2,2))
0,25	0,91	-148,69	27,09	95,00	0,01	5,77	0,38	-127,69
0,50	0,92	-165,28	13,51	76,92	0,01	-11,36	0,44	-137,97
0,75	0,92	-171,72	8,65	64,59	0,01	-22,78	0,52	-141,86
1,00	0,93	-175,64	6,14	54,40	0,01	-32,05	0,59	-145,72
1,25	0,94	-178,63	4,62	45,61	0,01	-39,93	0,66	-149,79
1,50	0,94	178,83	3,61	37,90	0,01	-46,72	0,71	-153,85
1,75	0,95	176,52	2,90	31,06	0,01	-52,63	0,76	-157,73
2,00	0,95	174,36	2,39	24,93	0,01	-57,82	0,79	-161,39
2,25	0,95	172,30	2,01	19,38	0,01	-62,41	0,82	-164,80
2,50	0,95	170,30	1,71	14,31	0,01	-66,50	0,84	-167,99
2,75	0,95	168,34	1,49	9,62	0,01	-70,19	0,86	-170,98
3,00	0,96	166,41	1,31	5,25	0,01	-73,54	0,87	-173,80
3,25	0,96	164,47	1,16	1,12	0,01	-76,60	0,89	-176,47
3,50	0,96	162,52	1,05	-2,80	0,01	-79,43	0,89	-179,02
3,75	0,96	160,54	0,95	-6,55	0,01	-82,05	0,90	178,51
4,00	0,96	158,52	0,88	-10,19	0,01	-84,50	0,91	176,12
4,25	0,96	156,45	0,81	-13,73	0,00	-86,79	0,92	173,78
4,50	0,96	154,30	0,76	-17,22	0,00	-88,96	0,92	171,47
4,75	0,96	152,08	0,72	-20,66	0,00	-91,02	0,92	169,17
5,00	0,96	149,76	0,68	-24,11	0,00	-92,97	0,93	166,87
5,25	0,95	147,32	0,66	-27,57	0,00	-94,82	0,93	164,55
5,50	0,95	144,75	0,63	-31,07	0,00	-96,58	0,93	162,19
5,75	0,95	142,02	0,62	-34,65	0,00	-98,24	0,93	159,79
6,00	0,95	139,11	0,60	-38,33	0,00	-99,80	0,93	157,31
6,25	0,95	136,00	0,60	-42,14	0,00	-101,22	0,93	154,75
6,50	0,94	132,64	0,59	-46,11	0,00	-102,48	0,93	152,09
6,75	0,94	129,02	0,59	-50,28	0,00	-103,53	0,93	149,30
7,00	0,93	125,07	0,60	-54,68	0,00	-104,28	0,93	146,36
7,25	0,93	120,75	0,61	-59,36	0,00	-104,62	0,93	143,24
7,50	0,92	116,00	0,62	-64,36	0,00	-104,38	0,93	139,92
7,75	0,91	110,75	0,64	-69,74	0,00	-103,37	0,92	136,34
8,00	0,90	104,91	0,66	-75,55	0,00	-101,32	0,92	132,48
8,25	0,89	98,38	0,69	-81,86	0,00	-98,03	0,91	128,27
8,50	0,87	91,03	0,72	-88,74	0,00	-93,52	0,90	123,65
8,75	0,85	82,74	0,75	-96,26	0,00	-88,27	0,89	118,54
9,00	0,84	73,35	0,79	-104,52	0,00	-83,34	0,88	112,83
9,25	0,81	62,72	0,83	-113,58	0,00	-80,00	0,86	106,41
9,50	0,79	50,71	0,87	-123,52	0,00	-79,12	0,85	99,12
9,75	0,77	37,27	0,91	-134,38	0,01	-81,00	0,83	90,77
10,00	0,76	22,46	0,94	-146,19	0,01	-85,50	0,81	81,14

phase(S(i,j)) in °

## Advanced Information

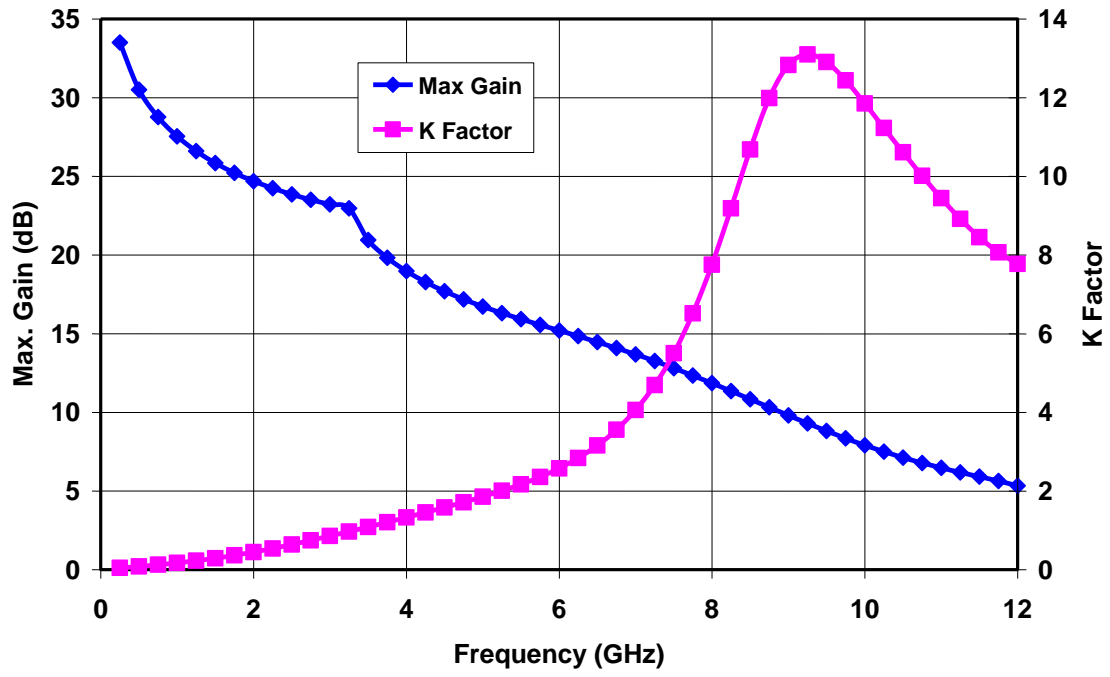
Ref. : AI1011182 – 01 Jul 11

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Maximum Gain & Stability Characteristics

T<sub>case</sub>= +25°C, CW mode, V<sub>D</sub>=50V, I<sub>D\_Q</sub>=300mA

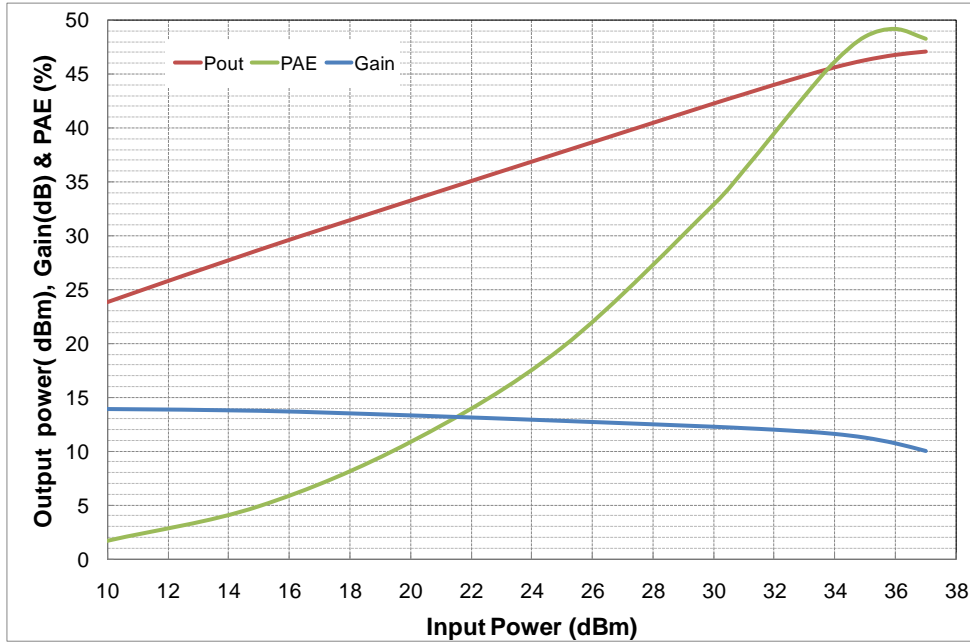


Advanced Information

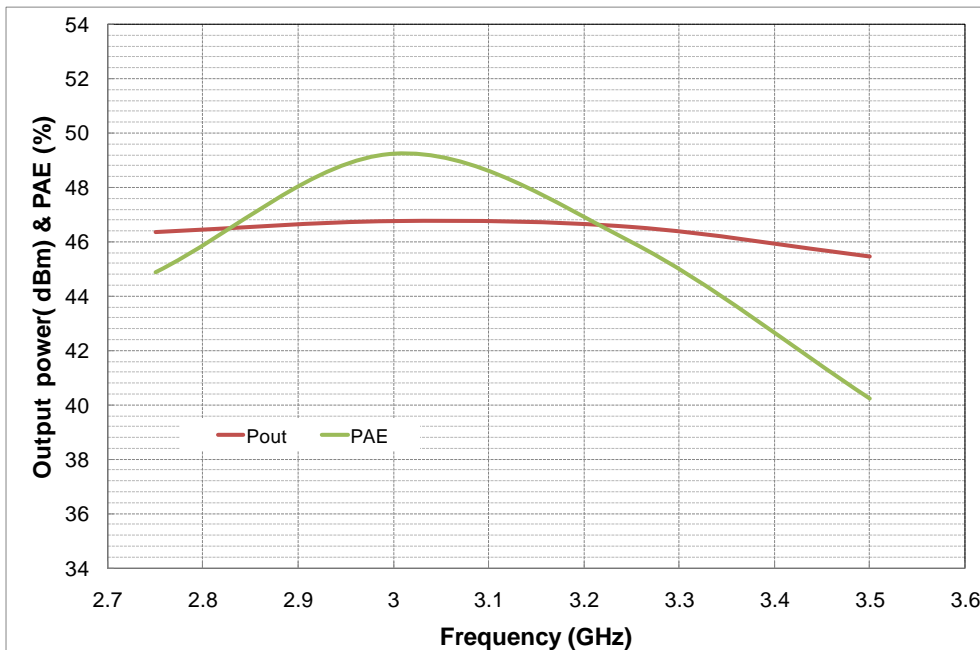
**Typical Performance on Demonstration Board (Ref. 61499547)**

Tcase = +25°C, CW mode,

Measured Pout, Gain & PAE  
 F = 3GHz, V<sub>DS</sub> = 50V, I<sub>D\_Q</sub> = 350mA



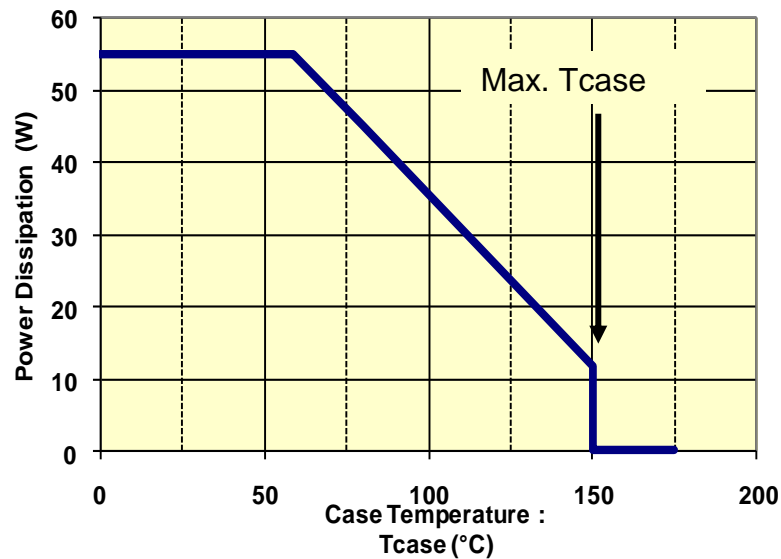
Measured Pout & PAE  
 Pin = 36dBm, V<sub>DS</sub> = 50V, I<sub>D\_Q</sub> = 350mA



Advanced Information

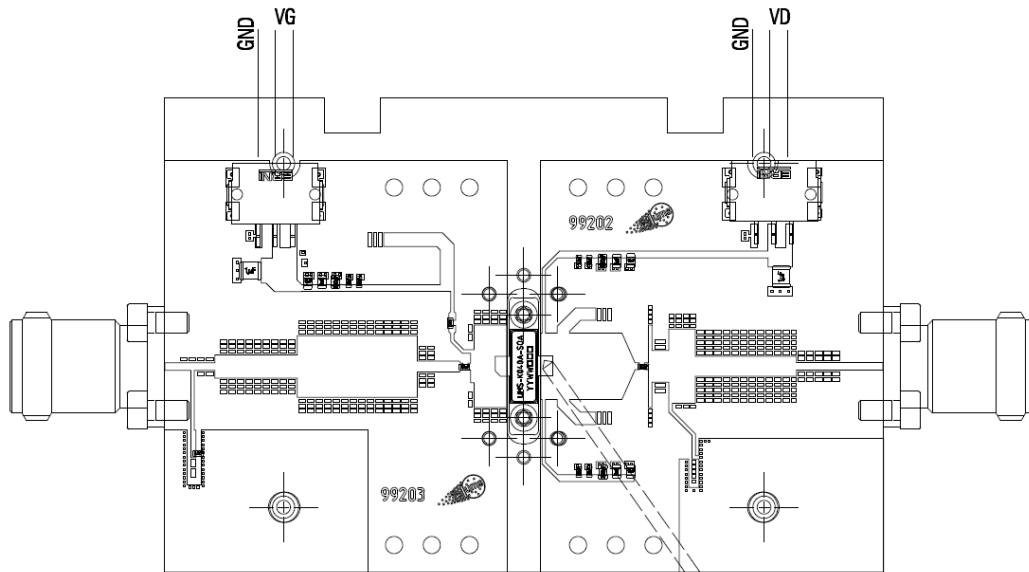
## Power Dissipation & Thermal Limitations

The CHK040A-SOA is packaged in a low thermal resistance power package. The maximum dissipated power for the device has to remain below to the limits indicated on the following graph. These limits are given as a function of the case temperature ( $T_{case}$ ). This temperature is measured at the center of the package's bottom side as shown at section "Package Outline". Case temperature ( $T_{case}$ ) has to remain lower than  $+150^{\circ}\text{C}$  which is the maximum allowed temperature for the package. This limit shall be considered for operating as well as for storage conditions.

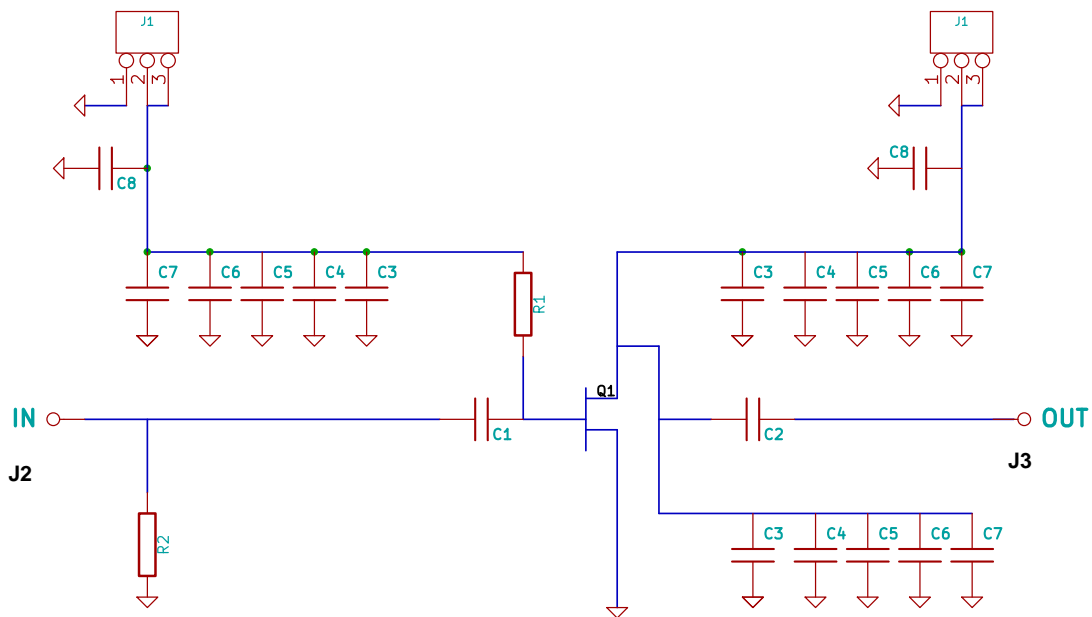


### Advanced Information

### Demonstration Amplifier Circuit Outline (Ref. 61499547)



### Demonstration Amplifier Low Frequency Equivalent Schematic (Ref. 61499547)

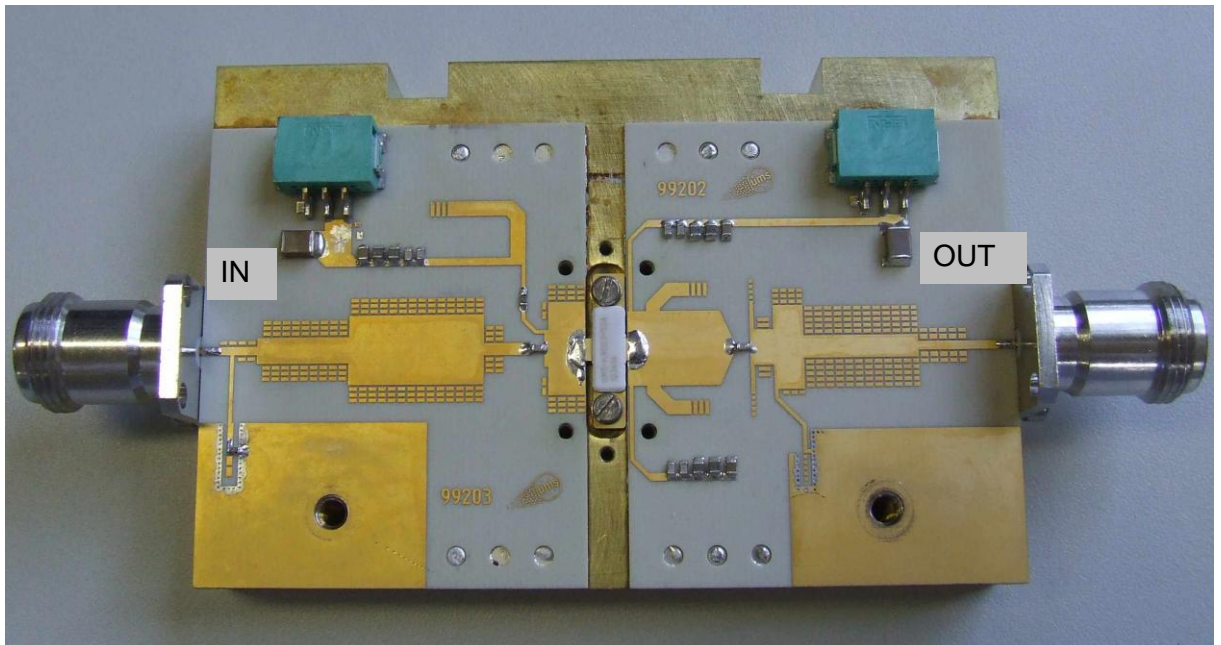


#### Advanced Information

## Demonstration Amplifier / Bill of Materials (Ref. 61499547)

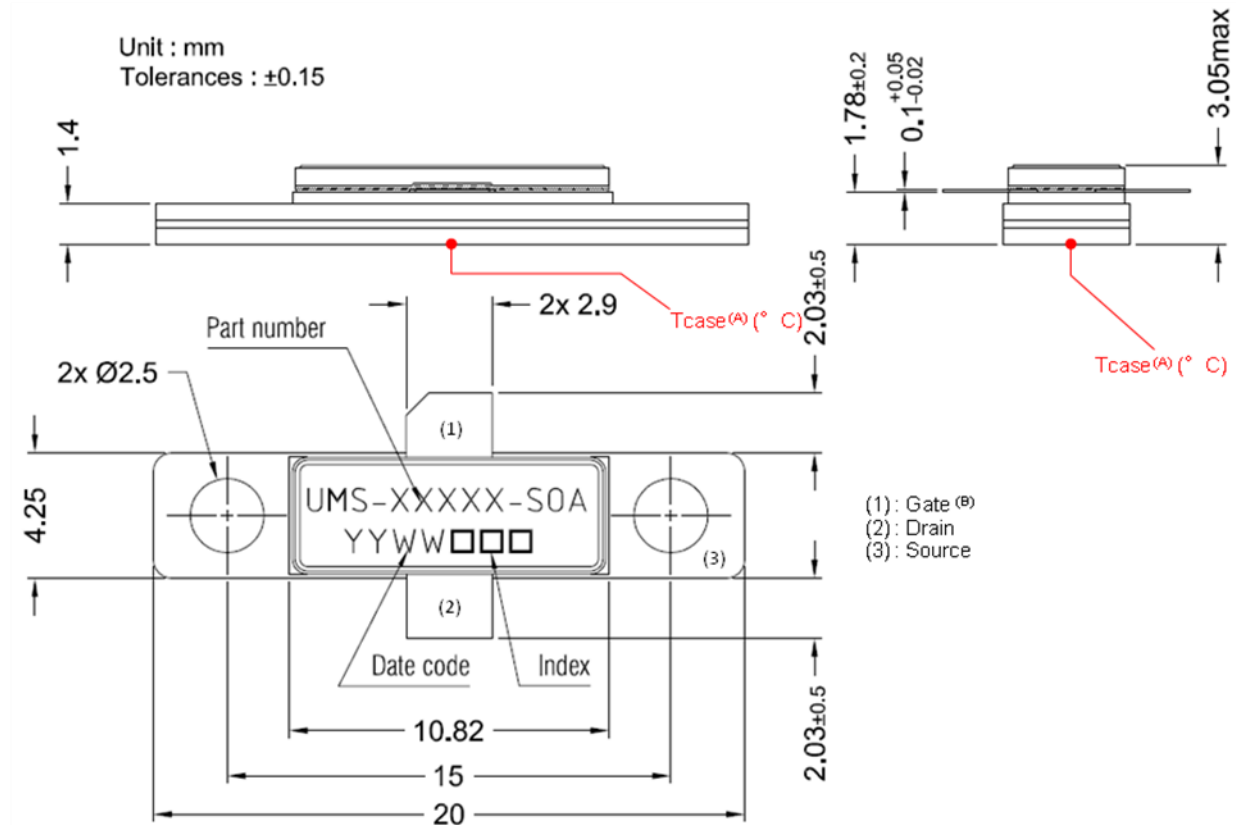
Designato	Type	Value - Description	Qty
C1	Capacitor	1.5pF, +/- 0.1pF, 0603	1
C2	Capacitor	2.7pF, +/- 0.1pF, 0603	1
C3	Capacitor	8.2pF, +/- 0.25%, 0603	3
C4	Capacitor	82pF, +/- 5%, 0603	3
C5	Capacitor	240pF, +/- 5%, 0805	3
C6	Capacitor	1nF, +/- 5%, 0805	3
C7	Capacitor	10nF, +/- 10%, 0805	3
C8	Capacitor	1 $\mu$ F, +/- 10%, 1812	2
R1	Resistor	22 $\Omega$ , +/- 1%, 0603	1
R2	Resistor	5 $\Omega$ , +/- 1%, 0603	1
J1	Connector	CMS 3cts	2
J2,J3	Connector	N DC-11GHz	2
Q1	Transistor	CHK040A-SOA	1

## Demonstration Amplifier Circuit (Ref. 61499547)



## Advanced Information

### Package outline



<sup>(A)</sup>  $T_{\text{case}}$  locates the reference point used to monitor the device temperature. This point has been taken at the device / system interface to ease system thermal design.

<sup>(B)</sup> Chamfered lead indicates the gate access of the transistor.

### Advanced Information

## Recommended Assembly Procedure

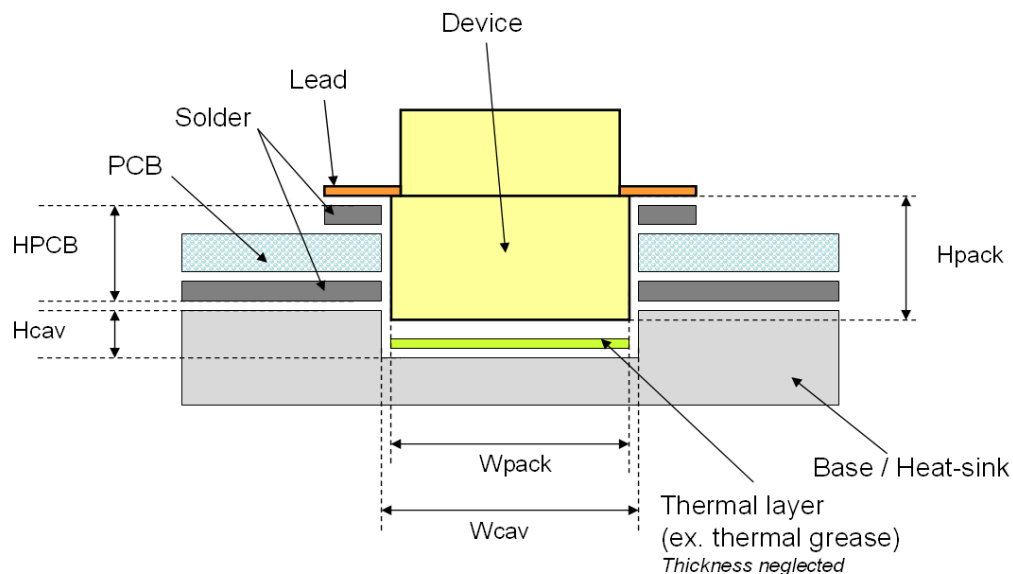
CHK040A-SOA is available has a flange package to be bolt down onto a thermal heat sink also used as main electrical ground. Use preferably screw M2 and flat washers.

Thermal and electrical resistance at the package to heat sink interface has to be as low as possible. Thermal electrically conductive grease or conductive thin layer like indium sheets are recommended between the package and the heat sink.

In case of a thermal grease is selected, we recommend to use material offering thermal conductivity  $>5\text{W/m.K}$  and electrical resistivity  $<0.01\text{ ohm.cm}$ . The grease layer thickness should be about  $25\mu\text{m}$  (1 mil).

Contact interface quality can be improved by cleaning process prior device mounting on the heat-sink. Such operation will enhanced the thermal and electrical contact by oxides removal at each interface.

Package leads can be soldered on printed circuit board's traces by using RoHS solder past. Cavity depth and width to be performed into the heat-sink where the device will be mounted are important to achieve the best performances. These dimensions have to be optimized in order to minimize the distance between device and signal traces made on the printed circuit board (PCB). But they also have to be calculated in order to accommodate device variations in height. The following drawing gives the relationship between device dimensions ( $H_{\text{pack}}$  &  $W_{\text{pack}}$ ) and optimal cavity depth ( $H_{\text{cav}}$ ) and width ( $W_{\text{cav}}$ ) depending on the printed circuit-board configuration ( $H_{\text{PCB}}$ ).



$$H_{\text{cav}} = (H_{\text{pack}_{\text{min}}} - H_{\text{PCB}_{\text{max}}})^{+0}_{-0.05}$$

$$W_{\text{cav}} = (W_{\text{pack}_{\text{max}}} + 0.4)^{+/- 0.05}$$

dimensions are in mm

## Advanced Information

### Recommended environmental management

Refer to the application note AN0019 available at <http://www.ums-gaas.com> for environmental data on UMS package products.

### Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Sampling request reference:  
Package : ES-CHK040A-SOA

#### Contact us

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